SEMICONDUCTOR RECESSED MASK INTERCONNECT TECHNOLOGY

ABSTRACT

A metal plus low dielectric constant (low-k) interconnect structure is provided for a semiconductor device wherein adjacent regions in a surface separated by a dielectric have dimensions in width and spacing in the sub 250 nanometer range, and in which reduced lateral leakage current between adjacent metal lines, and a lower effective dielectric constant than a conventional structure, is achieved by the positioning of a differentiating or mask member that is applied for the protection of the dielectric in subsequent processing operations, at a position about 2-5 nanometers below a, to be planarized, surface where there will be a lower electric field. The invention is particularly useful in the damascene type device structure in the art wherein adjacent conductors extend from a substrate through an interlevel dielectric material,connections are made in a trench, a diffusion barrier liner is provided in the interlevel dilectric material and masking is employed to protect the dilectric material between conductors during processing operations.